

Flip Chip Test Wafer Pac 2.0



- Wafer specifications
 - 6" silicon wafer
 - other substrates / semiconductor materials on request (e.g. glass, GaAs)

- General data

132 Chips		10 x 10 mm		
28 x	chip 1:	200 µm pitch	peripheral	184 I/O's
28 x	chip 2:	300 µm pitch	peripheral	120 I/O's
24 x	chip 3:	200/400 µm pitch	area	572 I/O's
24 x	chip 4:	250 µm pitch	staggered	248 I/O's
28 x	chip 5:	100 µm pitch	peripheral	376 I/O's

- Bump specifications

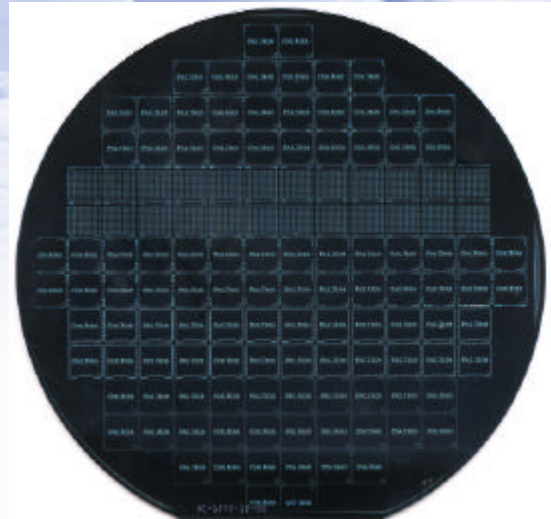
Available with following bump types

- Electroless Ni/Au (5µm, 10µm, 15µm and 25µm) for ACF, NCP and ICA adhesive Flip Chip attach
- Solder bumps
 - SnPb 63/37, SnAg4Cu0,5
 - other alloys on request (e.g. PbSn 90/10, AuSn 80/20)

- Electrical measurements

- Daisy Chain Structures
- Four Point Kelvin Structures

- For detailed information see www.pactech.de or www.pactech-usa.com (download designrules geometrical data FC Test Wafer Pac 2.0)



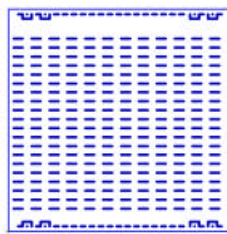
Prospekt Pac 2.0 03/2002



Chip 1



Chip 2



Chip 3



Chip 4



Chip 5

For information please look at our webpage www.pactech.de contact us:

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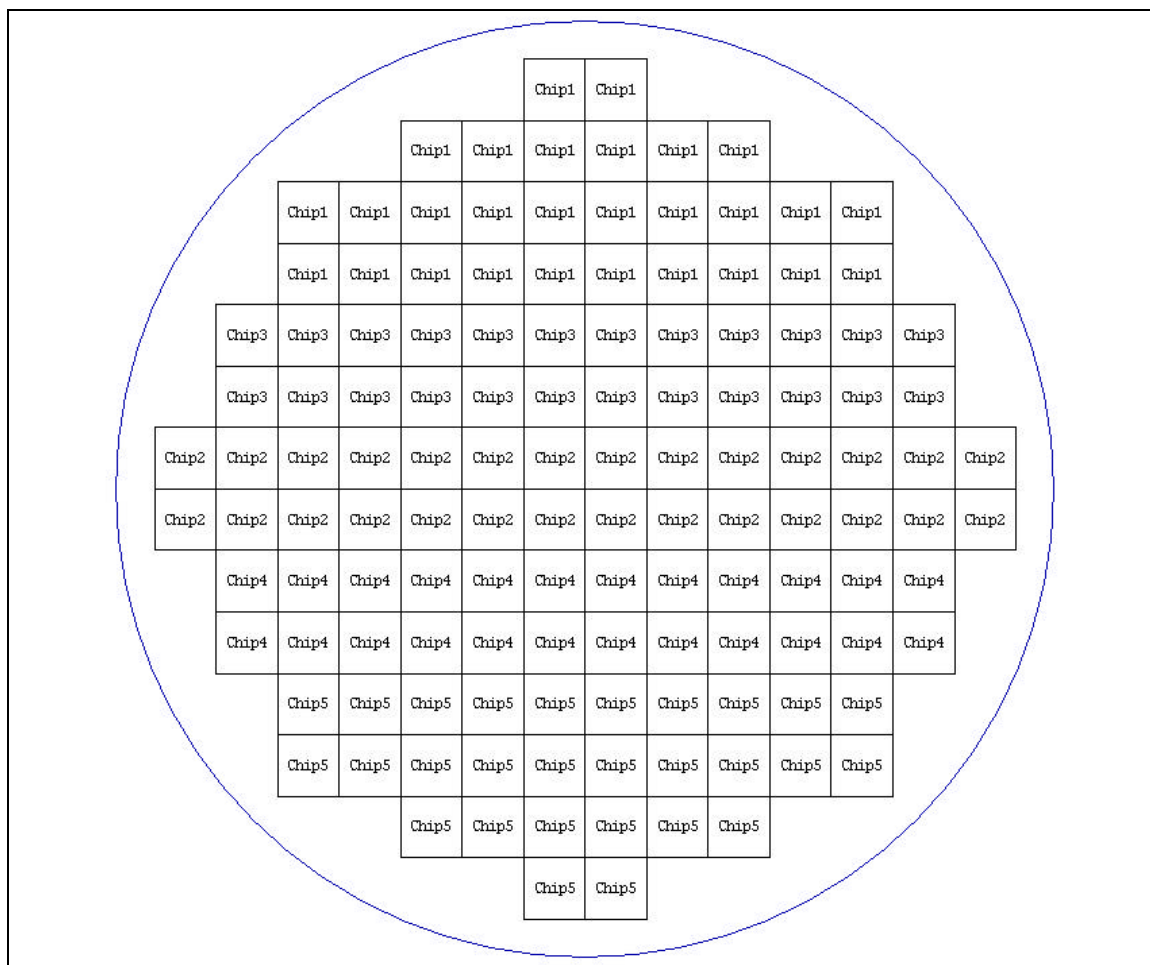
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Test Chips Specifications

1. General data

chip no	chip size / mm	pitch / μm	pad configuration	I/O's	chips per wafer
1	10,0 x 10,0	200	peripheral	184	28
2		300	peripheral	120	28
3		200/400	area	572	24
4		250	staggered	248	24
5		100	peripheral	376	28

2. Wafer mapping

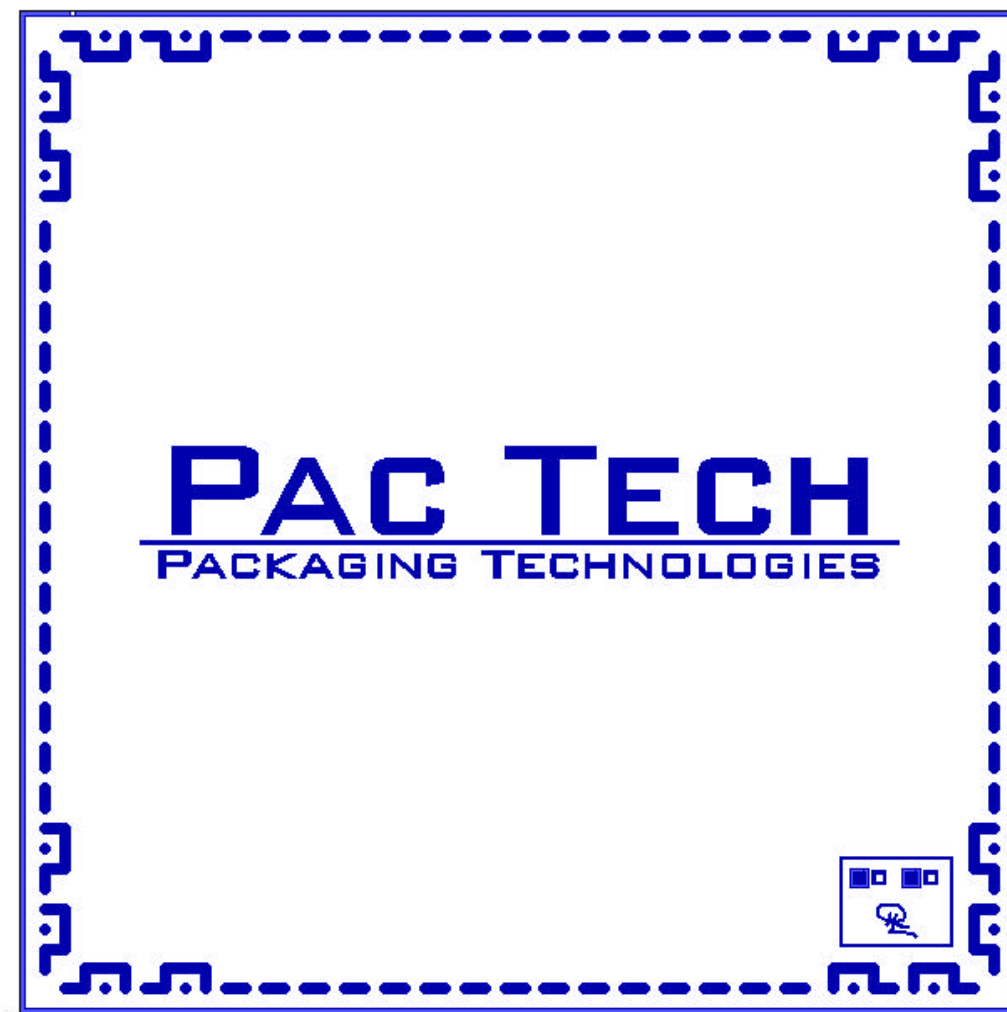


3.1 Chip documentation Pac 2.0

Chip 1	Chip size : 10 x 10 mm		
pitch	200 μm	Distance to Neural Point / DNP	7.071 mm
pad size	100 μm	symmetry	X, Y
passivation opening	80 μm	saw trace width	100 μm
bump size*	90 μm	dist. pad center to chip edge**	200 μm
pad configuration	peripheral	daisy chain structures	4 x 15
pad geometry	octagonal	four point Kelvin structures	4 x 4
number of pads	184 I/O's	alignment marks / FC	no
pad material	1 μm AlSi	alignment marks / lithography	yes

*size of Ni/Au UBM: 5 μm

**excluding saw trace

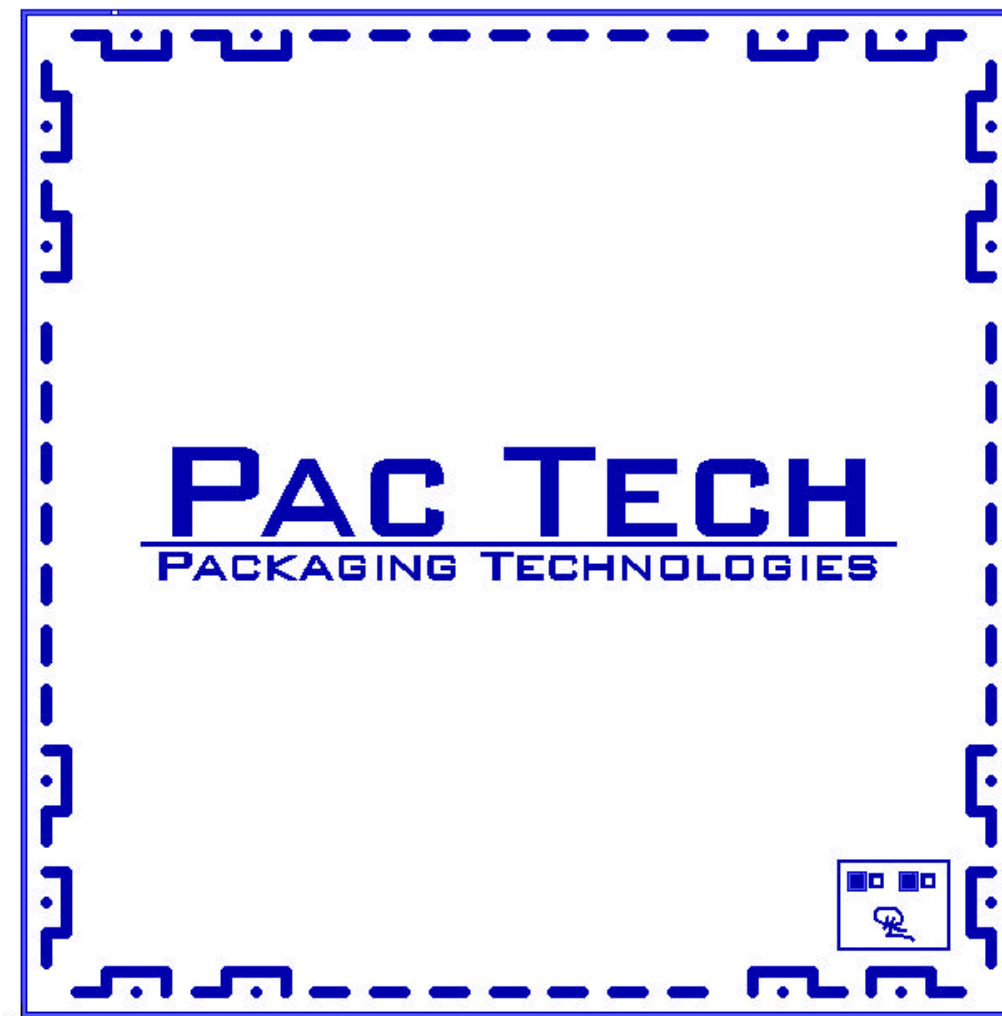


3.2 Chip documentation Pac 2.0

Chip 2	Chip size : 10 x 10 mm		
pitch	300 μm	Distance to Neural Point / DNP	7.071 mm
pad size	100 μm	symmetry	X, Y
passivation opening	80 μm	saw trace width	100 μm
bump size*	90 μm	dist. pad center to chip edge**	200 μm
pad configuration	peripheral	daisy chain structures	4 x 7
pad geometry	octagonal	four point Kelvin structures	4 x 4
number of pads	120 I/O's	alignment marks / FC	no
pad material	1 μm AlSi	alignment marks / lithography	yes

*size of Ni/Au UBM: 5 μm

**excluding saw trace

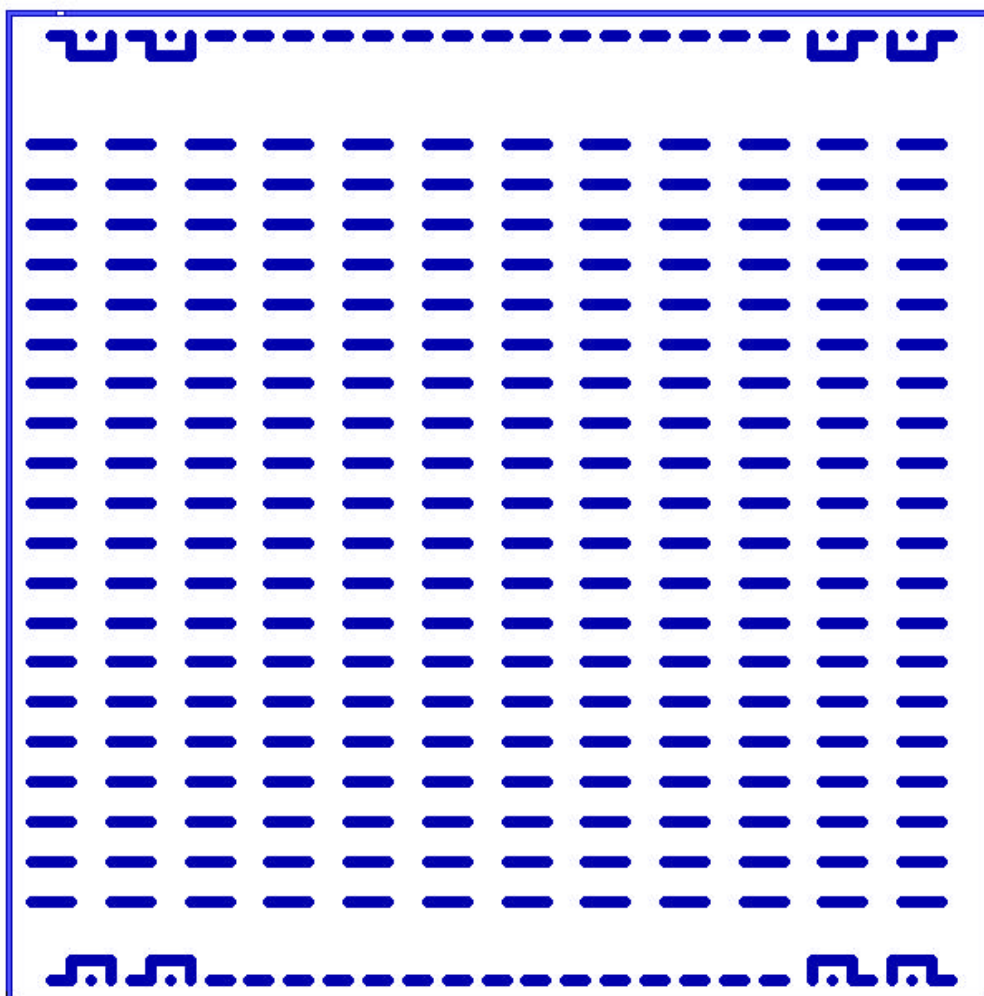


3.3 Chip documentation Pac 2.0

Chip 3	Chip size : 10 x 10 mm		
pitch	200/400 μm	Distance to Neural Point / DNP	7.071 mm
pad size	100 μm	symmetry	no
passivation opening	80 μm	saw trace width	100 μm
bump size*	90 μm	dist. pad center to chip edge**	200/500 μm
pad configuration	area	daisy chain structures	30 + 240
pad geometry	octagonal	four point Kelvin structures	4 x 2
number of pads	572 I/O's	alignment marks / FC	no
pad material	1 μm AISi	alignment marks / lithography	no

*size of Ni/Au UBM: 5 μm

**excluding saw trace



3.4 Chip documentation Pac 2.0

Chip 4	Chip size : 10 x 10 mm		
pitch	250 μm	Distance to Neural Point / DNP	7.071 mm
pad size	110 μm	symmetry	X
passivation opening	100 μm	saw trace width	100 μm
bump size*	110 μm	dist. pad center to chip edge**	235/450 μm
pad configuration	staggered	daisy chain structures	4 x 35
pad geometry	octagonal	four point Kelvin structures	-
number of pads	284 I/O's	alignment marks / FC	no
pad material	1 μm AlSi	alignment marks / lithography	yes

*size of Ni/Au UBM: 5 μm

**excluding saw trace



3.5 Chip documentation Pac 2.0

Chip 5	Chip size : 10 x 10 mm		
pitch	100 μm	Distance to Neural Point / DNP	7.071 mm
pad size	45 μm	symmetry	X, Y
passivation opening	27 μm	saw trace width	100 μm
bump size*	37 μm	dist. pad center to chip edge**	125 μm
pad configuration	peripheral	daisy chain structures	4 x 39
pad geometry	octagonal	four point Kelvin structures	4 x 4
number of pads	376 I/O's	alignment marks / FC	no
pad material	1 μm AlSi	alignment marks / lithography	yes

*size of Ni/Au UBM: 5 μm

**excluding saw trace

